

## MULTIPLE JUNCTION THIN FILM TRANSISTOR

### BACKGROUND

[0001] The present disclosure relates to technology for thin film transistors.

[0002] One use of a thin film transistor (TFT) is as a selection device. For example, the TFT can be used as a switch to electrically connect or disconnect two conductive regions. In this example, the source and drain of the TFT are connected to the respective two conductive regions. A control signal is applied to the gate of the TFT to control the electrical connection between the two conductive regions. This might be used to pass a signal from one conductive region to the other. As one particular example, a TFT selection device could be used to provide an electrical signal to a bit line in a non-volatile storage device. There are many other possible uses of a TFT.

### BRIEF DESCRIPTION OF THE DRAWINGS

[0003] FIG. 1 is an equivalent circuit of a portion of an example three-dimensional array of variable resistance memory elements, wherein the array has vertical bit lines.

[0004] FIG. 2 is a schematic block diagram of a re-programmable non-volatile memory system which utilizes the memory array of FIG. 1, and which indicates connection of the memory system with a host system.

[0005] FIG. 3 provides plan views of the two planes and substrate of the three-dimensional array of FIG. 1, with some structure added.

[0006] FIG. 4 is an expanded view of a portion of one of the planes of FIG. 3, annotated to show effects of programming data therein.

[0007] FIG. 5 is an expanded view of a portion of one of the planes of FIG. 3, annotated to show effects of reading data therefrom.

[0008] FIG. 6 is an isometric view of a portion of the three-dimensional array shown in FIG. 1 according to a first specific example of an implementation thereof

[0009] FIG. 7 is an equivalent circuit of a portion of an example three-dimensional array of variable resistance memory elements, wherein the array has vertical bit lines and a pillar select layer, both of which are above (and not in) the substrate.

[0010] FIG. 8A is a schematic that depicts a vertical bit line, a vertically oriented select device and a global bit line.

[0011] FIG. 8B is a plan view that depicts a vertical bit line, a vertically oriented select device and a global bit line.

[0012] FIG. 9 is a schematic of a portion of the memory system, depicting vertical bit lines above the substrate, vertically oriented select devices above the substrate and row select line drivers in the substrate.

[0013] FIG. 10 is a schematic diagram to illustrate some of the concerns pertaining to a TFT selection device.

[0014] FIGS. 11A and 11B depict various embodiments of vertical TFT selection devices.

[0015] FIG. 12A is a graph that depicts an affect that one embodiment of the second body region has on the electric field (e-field) of the TFT.

[0016] FIG. 12B shows curves of impact ionization rate versus location along the channel of one embodiment of the two TFTs discussed with respect to FIG. 12A.

[0017] FIG. 13A is a graph that shows doping concentration versus position for embodiments of a multiple junction TFT.

[0018] FIG. 13B is a graph that shows the e-field versus position for to show the effect of the thickness of the second body region for the embodiments of FIG. 13A.

[0019] FIG. 13C is a graph that shows the drain current ( $I_D$ ) versus the gate to source voltage ( $V_{gs}$ ) to show the effect of the thickness of the second body region for the embodiments of FIG. 13A.

[0020] FIG. 13D is a graph that shows the trans-conductance ( $g_m$ ) versus the gate to source voltage ( $V_{gs}$ ) to show the effect of the thickness of one embodiment of the second body region on  $g_m$ .

[0021] FIG. 13E is a graph that shows  $I_D$  versus the drain to source voltage ( $V_{ds}$ ) to show the effect of the thickness one embodiment of the second body region on the drain current ( $I_D$ ).

[0022] FIG. 13F is a graph that shows  $I_D$  versus the drain to source voltage ( $V_{ds}$ ) to show the effect of the thickness one embodiment of the second body region on the breakdown voltage.

[0023] FIG. 14A is a graph depicting three example peak doping concentrations for the second body region.

[0024] FIG. 14B is a graph depicting the e-field versus position to show the effect of the peak doping concentration of one embodiment of the second body region.

[0025] FIG. 14C is a graph depicting  $I_D$  versus  $V_{ds}$  to show the effect of the peak doping concentration of the one embodiment of the second body region on the breakdown voltage.

[0026] FIG. 15A is a cross-sectional view of a memory structure using one embodiment of a multiple junction vertically oriented TFT select device and the memory structure of FIG. 6.

[0027] FIG. 15B is a cross-sectional view of another embodiment of a memory structure using the vertically oriented TFT select device and the memory structure of FIG. 6.

[0028] FIG. 16 is a partial schematic of the memory system of FIGS. 15A and 15B, depicting the above-described double-gated structure for the vertically oriented TFT select devices.

[0029] FIG. 17 shows another partial schematic also depicting one embodiment of the double-gated structure.

[0030] FIG. 18 is a flow chart describing one embodiment for manufacturing a Pillar Select Layer having a vertical TFT selected device.

[0031] FIGS. 19A-19E depict results after various steps of one embodiment of FIG. 18.

[0032] FIG. 20A is one embodiment of a process of doping the various silicon layers that form the source/drains and body of the TFT.

[0033] FIGS. 20B-20C depict results after various steps of one embodiment of FIG. 20A.

[0034] FIG. 21A is a flowchart of another embodiment for doping the various layers in the TFT 504.

[0035] FIG. 21B roughly shows rough concentrations for the one step implant of the process of FIG. 21A.

[0036] FIG. 22A is a flowchart of another embodiment for doping the various layers in the TFT.

[0037] FIGS. 22B-22C depict results after various steps of one embodiment of FIG. 22A.